

Proposal and Analysis of a Five-level Unidirectional Totem-Pole PFC Rectifier for Electric Vehicle On-board Charger

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Abstract— The growing demand for electric vehicles and the constraints of this application have driven the development of high-performance power electronic converters. On-board chargers (OBCs), typically built with a two-stage architecture (high power factor rectifier + dc-dc converter), play an important role in this scenario. Nevertheless, challenging metrics such as power density, specific power and efficiency are posed to high-performance OBCs design. This paper presents the development of a five-level unidirectional high power factor single-phase rectifier, based on a totem-pole topology employing multi-state switching cells concepts. Operation, modulation scheme, input current analysis, evaluation of semiconductor losses are presented. Finally, simulation results and details of a 6.6 kW converter are presented and discussed.

Index Terms—High efficiency, power factor correction, PWM rectifiers, multistate switching cells, on-board chargers, electric vehicle.

I. INTRODUCTION

An increasing demand for electric vehicles (EVs) has been observed in the last decades. In fact, several countries and car manufactures have adopted policies and goals concerning the reduction of fossil-fueled vehicles, fleet renewal with electric vehicles, environmental issues, and so on. In order to supply such demand, power electronic converters are needed, such as inverters, on board battery chargers and dc-dc converters to provide power for the low voltage battery from the high voltage battery. Furthermore, these converters must meet particular constraints of EVs. According to [1], the *US DRIVE Partnership* set power electronics targets for 2025 concerning EVs. Particularly, for OBCs the cost of 35 \$/kW, specific power of 4 kW/kg, 4.6 kW/L for power density and efficiency of 98% are presented.

Apart of well know challenges concerning EVs (battery cell technology, charging infrastructure, range anxiety, etc.) the high cost is a paramount issue for several consumers. In

this scenario, the conversion of internal combustion engine vehicles (ICEV) to EV is seem as a promising alternative to the high cost of commercially available EVs. Thus, the needed of high performance power electronic converters for EVs can be even more expressive in the short term. The main task of the OBCs is to manage the electrical energy flow from the grid to the high voltage battery. Currently, bidirectional OBCs have attracted attention because new possibilities as vehicle-to-grid (V2G), vehicle-to-home (V2H), vehicle-to-load (V2L) and vehicle-to-vehicle (V2V) are enabled with a bidirectional power flow. On the other hand, unidirectional OBCs are simpler and meet the basic needs of charge. Unidirectional OBCs are typically built with a two-stage architecture, where a high power factor rectifier is employed to comply with the grid harmonic requirements, whereas a dc-dc converter controls the battery charge.

This work presents the development of a five-level unidirectional single-phase power factor correction (PFC) rectifier to be employed in on-board chargers of EVs. A topology based on a totem-pole rectifier employing multi-state switching cells concepts is proposed as a candidate to meet high levels of efficiency, power density and specific power.

II. FIVE-LEVEL UNIDIRECTIONAL TOTEM-POLE PFC RECTIFIER

Various PFC rectifier topologies have been proposed in the last decades [2], [3], covering different applications. In particular, single-phase PFC rectifiers for OBCs typically process significant power levels (e.g 6.6 kW - level 2) and operate with large input voltage range. Furthermore, high efficiency, low weight and small volume, among other requirements, are typically required in such applications. In this sense, topologies with reduced conduction and switching losses, as well the ability to manage high current levels are desired.

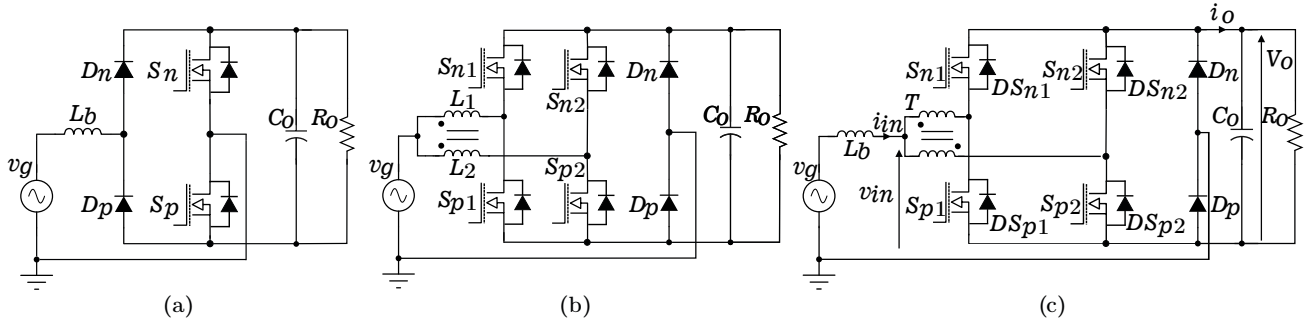


Fig. 1. Different bridgeless single-phase PFC rectifiers: (a) Totem-pole PFC rectifier (b) Two-channel interleaved totem-pole PFC rectifier; (c) Proposed two-channel totem-pole PFC rectifier with multi-interphase transformer.

Several PFC topologies have been discussed in the recent years for OBCs [3], [5], [6].

The totem-pole bridgeless PFC rectifier [7] shown in Fig.1 (a) has attracted attention for OBCs [8]–[10], mainly after the commercial availability of high performance power devices employing large bandgap semiconductor materials (Silicon Carbide - SiC and Gallium Nitride-GaN). High switching frequencies are possible, along to reduced conduction losses. On the other hand, interleaving and multistate switching cells concepts are adequate to electrical energy processing with high current levels. A two-channel interleaved totem-pole boost bridgeless PFC rectifier is introduced in [11] and shown in Fig.1 (b). The converter employs two coupled inductors for input current sharing and focuses on an operating scheme to reduce reverse-recovery problems, since conventional silicon MOSFETs are utilized. In [12], [13], current sharing, multilevel operation and frequency multiplication are naturally achieved with the multistate switching cells concepts, enabling smaller electromagnetic compatibility filter components. The converter proposed in this work is shown in Fig.1-(c) and brings together the benefits of basic totem-pole converter and the multi-state switching cell concepts.

A. Basic operation and modulation scheme

As shown in Fig.1(c), the converter employs two magnetic devices, a conventional boost inductor and a multi-interphase transformer, which dictates the overall converter operation and main waveforms.

The general modulation scheme employs two π rad displaced carriers (triangular or sawtooth), which are compared with a modulation signal generated by the current controller. Thus, the respective signals of each leg are displaced by π rad of each other. Fig. 2 illustrates hypothetical carriers, modulation and gate signals for the aforementioned modulation scheme.

For high power factor operation, the modulation signal for both legs are approximate with

$$d(\theta) = 1 - M |\sin(\theta)|, \quad (1)$$

where M is the modulation index, given by $M = \hat{V}_g/V_o$, \hat{V}_g is the grid peak voltage and V_o is the nominal output voltage.

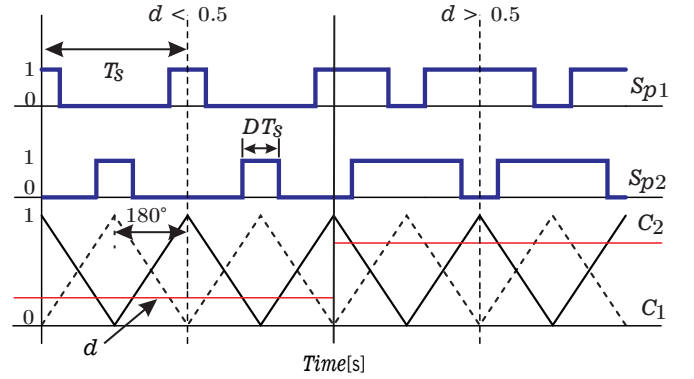


Fig. 2. Exemplary command signals for the switches S_{p1} and S_{p2} , generated from a comparison of the modulation signal d with two displaced carriers C_1 e C_2 .

As the operation is symmetrical for both mains half-cycles, an additional logic or software scheme must guarantee that the switches S_{p1} and S_{p2} are the active devices for the positive mains half-cycle, whereas S_{n1} and S_{n2} are the active devices in the negative mains half-cycle. The diodes D_n and D_p operate at the grid frequency and impose the unidirectional feature of the converter. In a more conventional scenario, the active semiconductors of the same leg are driven with complementary PWM signals and a proper dead time is required in order to avoid the shoot-through. This allows additional benefits in terms of conduction losses when MOSFETs are employed (third quadrant operation). Fig. 3 presents modulation signals for the positive and negative switches groups.

The converter operating stages depends basically on the input current polarity and the command signals of the active switches. Similarly to presented in [12], different operation stages occurs according to the modulation index M .

Fig.4 illustrates the four operating stages, when the converter operates at the positive mains half-cycle and continuous conduction mode. Since the converter operation is symmetrical, for the sake of brevity the operation at the negative mains half-cycle will be not presented. From (1), if $M < 0.5$, the instantaneous duty cycle $d(\theta)$ is always greater than 0.5, and thus there is an overlapping of the command signals (see Fig. 2). In such case, the operating stages for the positive grid half-

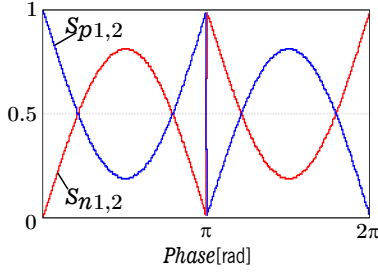


Fig. 3. Modulation signals for the positive grid half-cycle active devices (S_{p1} and S_{p2}) and for negative grid half-cycle devices (S_n). The signals are complementary and, thus, a synchronous rectification is achieved.

cycle are sequentially IV-III-IV-II, illustrated in Fig.4. On the other hand, for $M > 0.5$, the operating stages differ according to the instantaneous duty cycle. If $d(\theta) < 0.5$, there are not command overlap and the operating stages are sequentially II-I-III-I. When $d(\theta) > 0.5$, the operating stages are sequentially IV-III-IV-II again.

The multi-interphase transformer plays an important role on the converter waveforms generation. The general operation of the multi-interphase transformer is presented in [12]. According to the active switches states (on or off), the converter presents up to five voltage levels at v_{in} . From the operating stages of Fig.4, three-levels are achieved if $M < 0.5$ and five-levels are possible if $M > 0.5$, as illustrated in Fig.5. It should be noted that the theoretical voltage across all semiconductor devices is always the output voltage v_o .

In addition to the multilevel generation of the input voltage, the first group of the high frequency content at v_{in} is twice the switching frequency, which contributes to an input filter reduction.

B. Control

From the external point of view, the presented converter is similar to other boost unidirectional PFC rectifiers. Thus, different control strategies and design methodologies are possible. However, a conventional two loop (outer voltage control loop and an inner current control loop) scheme is utilized here, in order to achieve high power factor at the input side and voltage regulation at the output side.

C. Input Current Ripple

Considering a sinusoidal grid voltage, the input voltage v_{in} is the source of high frequency content of the input current, which must be limited by the boost inductor L_b . Thus, the normalized input current ripple $\Delta \bar{i}_{in}$ is determined from the converter operating stages (Fig. 4) and respective waveforms (Fig. 5) according to

$$\Delta \bar{i}_{in}(M, \theta) = \left[M \sin(\theta) + \frac{\gamma(\theta) - 1}{2} \right] \left[1 - M \sin(\theta) - \frac{\gamma(\theta)}{2} \right] \quad (2)$$

with a normalization defined by

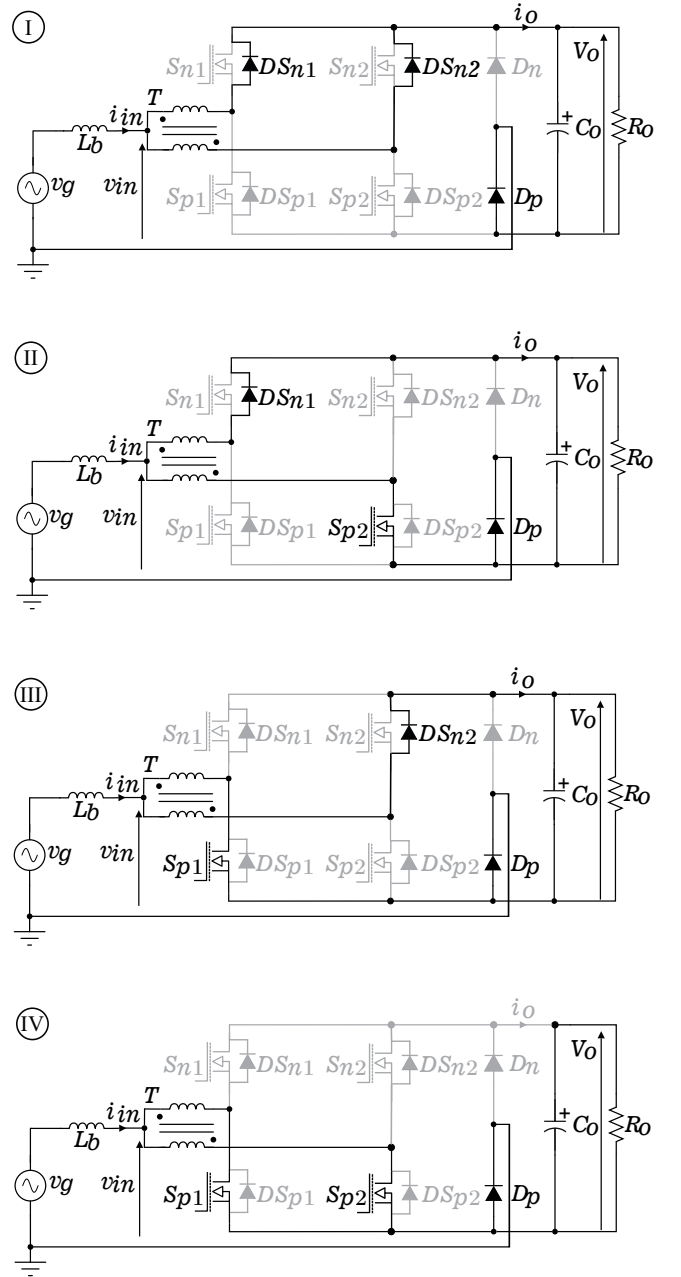


Fig. 4. Rectifier operating stages for the positive mains half-cycle, when: (I) $S_{p1} = 0$ and $S_{p2} = 0$; (II) $S_{p1} = 0$ and $S_{p2} = 1$; (III) $S_{p1} = 1$ and $S_{p2} = 0$; (IV) $S_{p1} = 1$ and $S_{p2} = 1$.

$$\Delta \bar{i}_{in} = \frac{\Delta i_{in} f_s L_b}{V_o}, \quad (3)$$

where Δi_{in} is the input current ripple, f_s is the switching frequency and the converter operating range $\gamma = 0$ for $d(\theta) < 0.5$ and $\gamma = 1$ for $d(\theta) > 0.5$. The graphical representation of (2) is presented in Fig.6. The normalized current ripple profile is clearly dependent of instantaneous phase θ and the modulation index M , but the maximum value $\Delta \bar{i}_{in} = 0.0625$, however, is constant for a large range of M .

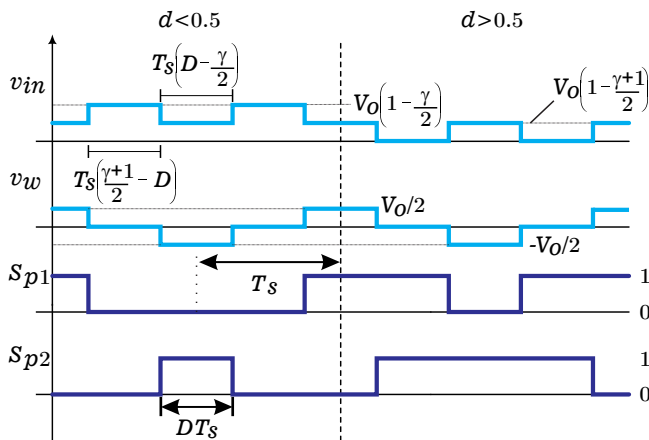


Fig. 5. Theoretical input voltage v_{in} and voltage across the multi-interphase transformer winding v_w , related to the active devices signals during positive grid half-cycle.

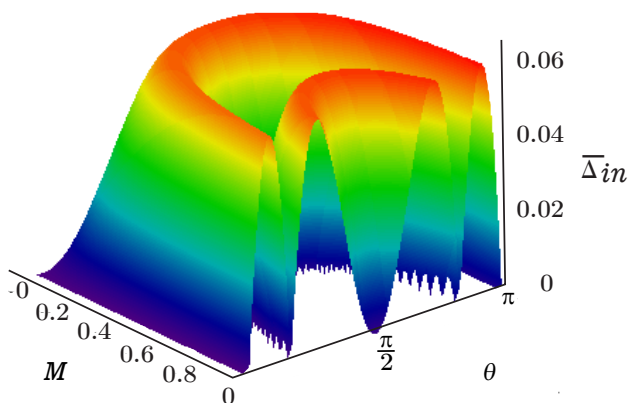


Fig. 6. Normalized input current ripple as a function of the instantaneous phase θ and the modulation index M .

III. SEMICONDUCTORS CURRENT EFFORTS AND LOSSES EVALUATION

Since the converter operates with large grid voltage range, the current efforts are dependent on the modulation index M . As previously stated, the converter consists of two high-frequency legs (MOSFETs) and one low-frequency leg (diodes). Considering the symmetric operation of the converter legs, as well the current sharing provided by the multi-interphase transformer, all MOSFETs experience the same current efforts. Similarly, the low-frequency diodes have equal current levels. Thus, in the following, the average and RMS current values will be determined only for devices operating at the positive half-cycle. Furthermore, the MOSFET channel and body diode are treated as separate devices, i.e., the synchronous rectification scheme (third quadrant operation) are not considered here.

The average and RMS current levels for the diodes DS_{nj} (with $j = 1, 2$) are obtained respectively with

$$IDS_{nj,avg} = \frac{1}{2\pi} \left[\int_0^\pi \frac{i_{in}(\theta)}{2} [1 - d(\theta)] d\theta \right], \quad (4)$$

and

$$IDS_{nj,rms} = \sqrt{\frac{1}{2\pi} \left[\int_0^\pi \left(\frac{i_{in}(\theta)}{2} \right)^2 [1 - d(\theta)] d\theta \right]}. \quad (5)$$

For the MOSFETs S_{pj} , the average and RMS current levels are respectively given by

$$IS_{pj,avg} = \frac{1}{2\pi} \int_0^\pi \frac{i_{in}(\theta)}{2} d(\theta) d\theta, \quad (6)$$

and

$$IS_{pj,rms} = \sqrt{\frac{1}{2\pi} \int_0^\pi \left(\frac{i_{in}(\theta)}{2} \right)^2 d(\theta) d\theta}. \quad (7)$$

Finally, the average and RMS levels for the diode D_p are calculated respectively with

$$ID_{p,avg} = \frac{1}{2\pi} \int_0^\pi i_{in}(\theta) d\theta \quad (8)$$

and

$$ID_{p,rms} = \sqrt{\frac{1}{2\pi} \int_0^\pi i_{in}(\theta)^2 d\theta}. \quad (9)$$

A closed solution for all semiconductor current efforts is obtained solving (4) to (9) and is shown in Table III. A strong dependency of the modulation index M is observed in the current efforts, except for the devices D_p and D_n . Furthermore, it should be noted that the peak input current \hat{i}_{in} is dependent on the modulation index too.

In order to evaluate the semiconductors current efforts, all average and RMS currents have been normalized respect to the average output current I_o and presented in Fig.7. As can be seen, high current efforts occur at low modulation indexes, which complicates the design of a full power converter for any grid voltage. In fact, some commercially available OBDs do not operate at full output power under all grid voltage conditions, since the input current is limited. Therefore, a power derating has been implemented to enable operation at maximum power with high modulation indexes, while still allowing for some degree of design optimization. Here, the full power is delivered for $200 \text{ V} < V_g < 230 \text{ V}$ (i.e. $0.74 < M < 0.86$), and is linearly reduced with a second point in 50% of the nominal output power for $V_g = 127 \text{ V}$, when ($M = 0.47$).

A. Semiconductor Losses Evaluation

Both conduction and switching losses can be estimated from the devices data sheets, according to the methodology presented in [14].

The conduction losses of the MOSFETs $S_{p,n}$, body diodes $DS_{p,n}$ and low frequency diodes $D_{p,n}$ are respectively given by

$$PS_{p,n,con} = \frac{1}{2\pi} \int_0^\pi \frac{i_{in}(\theta)}{2} d(\theta) v_{ds} \left[\frac{i_{in}(\theta)}{2} \right] d\theta, \quad (10)$$

TABLE I
AVERAGE AND RMS CURRENT EFFORTS IN ALL SEMICONDUCTORS, WITH
 $j = 1, 2$.

Device	Average Current	RMS Current
DS_{nj}, DS_{pj}	$\frac{\hat{i}_{in} \cdot M}{8}$	$\frac{\hat{i}_{in}}{2} \sqrt{\frac{2M}{3\pi}}$
S_{nj}, S_{pj}	$\frac{\hat{i}_{in}}{8\pi}(4 - M\pi)$	$\frac{\hat{i}_{in}}{2} \sqrt{\frac{1}{4} - \frac{2M}{3\pi}}$
D_n, D_p	$\frac{\hat{i}_{in}}{\pi}$	$\frac{\hat{i}_{in}}{2}$

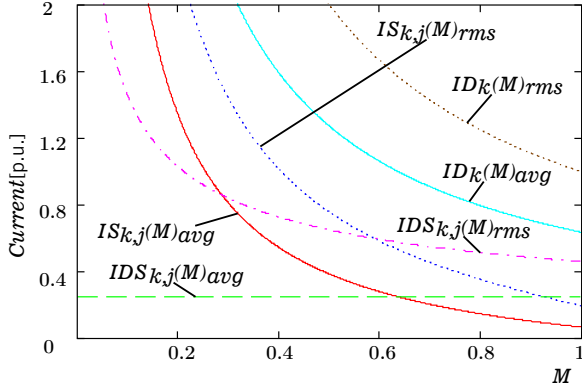


Fig. 7. Normalized current efforts across the semiconductor devices as a function of the modulation index, with $k = p, n$ and $j = 1, 2$.

$$PDS_{p,n,con} = \frac{1}{2\pi} \int_0^\pi \frac{i_{in}(\theta)}{2} [1 - d(\theta)] v_{ak} \left[\frac{i_{in}(\theta)}{2} \right] d\theta, \quad (11)$$

and

$$PD_{p,n,con} = \frac{1}{2\pi} \int_0^\pi \frac{i_{in}(\theta)}{2} v_{ak} \left[\frac{i_{in}(\theta)}{2} \right] d\theta, \quad (12)$$

where v_{ds} and v_{ak} represents the voltage across the MOSFETs and diodes, respectively. These current-dependent voltages can be obtained from the respective device datasheet.

On the other hand, the overall MOSFET switching losses are calculated with

$$PS_{com} = \frac{4f_s}{\pi} \int_0^\pi W_s \frac{i_{in}(\theta)}{2} d(\theta), \quad (13)$$

where W_s is the total switching energy (sum of the turn-off and turn-on energies), obtained from the clamped inductive switching energy vs. drain current graph presented in datasheets.

As diodes D_p and D_n operate at the grid frequency, their switching losses are negligible.

IV. RESULTS

The presented analyses have been validated with closed-loop simulations, related to a 6.6 kW prototype currently under construction. Table II presents the main specifications and devices of the prototype.

The main converter waveforms are respectively presented in Fig. 8(a) and Fig. 8(b) for two different modulation indexes,

TABLE II
MAIN DESIGN SPECIFICATIONS AND DEVICES OF THE 6.6 kW FIVE-LEVEL
UNIDIRECTIONAL TOTEM-POLE PFC RECTIFIER PROTOTYPE.

Specification / Device	Value / Description
Grid voltage	85-240 V, 60 Hz
Output voltage	380 V
Maximum output power	6.6 kW
Switching Frequency	40 kHz
Controller	TMS320F28069M
External communication	CAN
MOSFETs $S_{p1,2}$ and $S_{n1,2}$	SiC C3M0045065D, 49 A, 650 V
Diodes D_p and D_n	Silicon, RURG8060-F085, 80 A, 600 V

TABLE III
COMPARISON OF THE THEORETICAL AND SIMULATED SEMICONDUCTOR
CURRENT EFFORTS FOR $M = 0.82$, WITH $k = p, n$ AND $j = 1, 2$.

Device current stress	Theoretical [A]	Simulated [A]	Error [%]
$IDS_{kj,avg}$	4.34	4.3	0.98
$IDS_{kj,rms}$	8.84	8.81	0.32
$IS_{kj,avg}$	2.41	2.42	0.41
$IS_{kj,rms}$	5.86	5.91	0.86
$ID_{k,avg}$	13.5	13.44	0.45
$ID_{k,rms}$	21.21	21.18	0.16

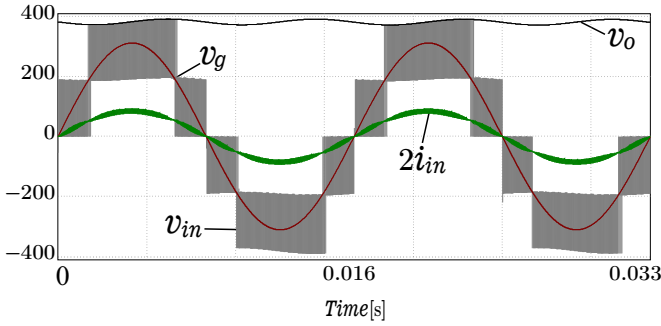
$M = 0.82$ and $M = 0.47$. In both cases, a high power factor operation is observed at the grid side, whereas a regulated output voltage is achieved at the output dc side. Furthermore, as previously explained, the input voltage waveform is dependent on the modulation index. From Fig. 8(a) and Fig. 8(b), it is clear that the input voltage presents five-levels and three-levels, respectively.

The normalized ripple envelope defined by (2) is compared to a normalized simulation with good agreement in Fig. 6. It should be noted that the theoretical current ripple is defined for peak-to-peak values, thus the comparison is carried out with $\Delta \bar{i}_{in}/2$.

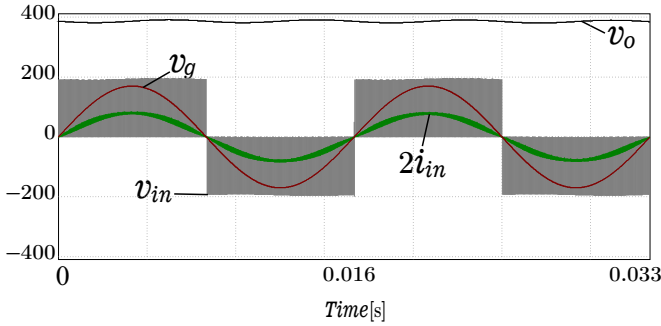
Table III presents a comparison of the theoretical and simulated semiconductor current efforts. The average and RMS current levels are presented for all semiconductors when the converter operates at full power and $V_g = 220$ V. Negligible errors are observed when comparing theoretical and simulation results.

A theoretical evaluation of the converter efficiency considering all estimated semiconductor losses is presented in Fig. 10. As can be seen, neglecting all other losses, a high efficiency is possible for a large output power range. Furthermore, the implemented power derating scheme guarantees high-efficiency operation over a wide grid voltage range, at the cost of reduced output power when $M < 0.74$.

Finally, a 3D projection of the designed and currently in construction prototype is provided in Fig. 11.



(a)



(b)

Fig. 8. Closed loop simulations of the presented PFC rectifier: grid voltage v_g , scaled input current $2i_{in}$, output voltage v_o and multilevel input voltage v_{in} for two different situations: (a) $V_g = 220\text{V}$ ($M = 0.82$) and ; (b) $V_g = 120\text{V}$ ($M = 0.45$).

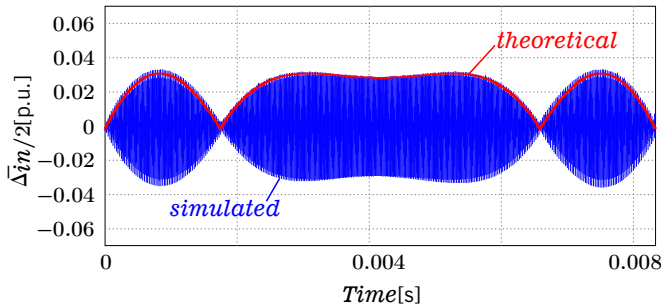


Fig. 9. Simulated and theoretical normalized input current ripple for $M = 0.82$.

V. CONCLUSION

A five-level totem-pole PFC rectifier has been proposed in this paper as a candidate for the front end stage of single-phase unidirectional onboard chargers. The converter takes benefits of current sharing, multilevel operation and frequency multiplication of the multistate switching cells concepts, and the low conduction losses of hard switching totem-pole topology enabled by high performance Silicon Carbide MOSFETs. General operation, modulation scheme and control aspects were introduced. An analysis of input current ripple was carried out, as well the semiconductor current efforts and losses evaluation. The carried out studies have been validated by consistent simulation results. The ability to operate with

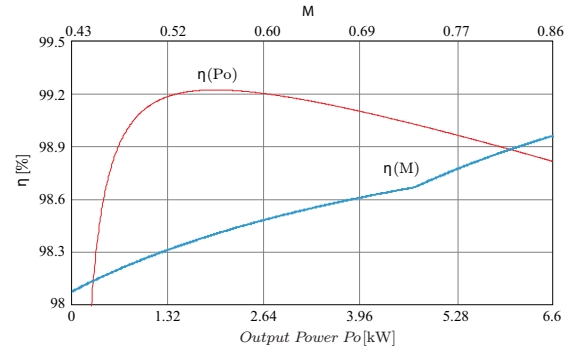


Fig. 10. (a) Theoretical efficiency as a function of the output power $\eta(P_o)$ (for $V_g = 220\text{V}$) and as a function of the modulation index $\eta(M)$.

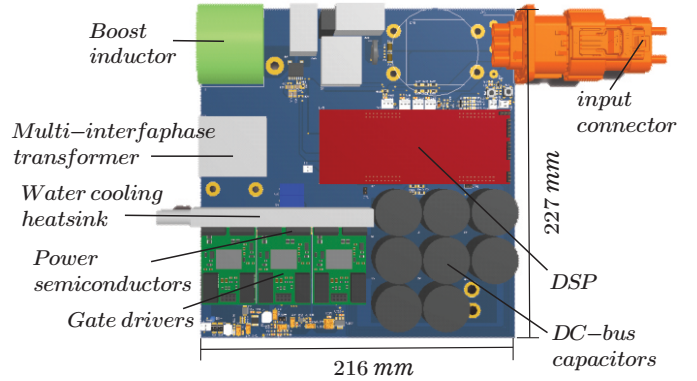


Fig. 11. Preliminary 3D picture of the prototype.

high input currents, low semiconductor losses, and the potential for reducing input filters make the converter suitable for integrating OBCs. A 6.6 kW prototype is currently under construction, and its results will be presented in future works.

ACKNOWLEDGMENT

The authors would like to thank Centrais Elétricas de Santa Catarina S.A (CELESC P&D) and the Brazilian Company of Research and Industrial Innovation (EMBRAPPI) for the financial support of Project PD-05697-0219/2019, titled "Inserção de Veículos Elétricos em Frotas Públicas, através da Conversão de Veículos a Combustão para Tração Elétrica", developed under the Research and Development program of the National Electric Energy Agency (ANEEL R&D).

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